WHAT IS CLAIMED IS:

1. A system for estimating the performance of an integrated circuit in a register transfer level, in which the performance of an integrated circuit is estimated based on a logic description of a register transfer level of the integrated circuit, the system for estimating the performance of an integrated circuit in a register transfer level comprising:

a library storing therein a device model for configuring the integrated circuit;

RTL description inputting means for inputting the logic description and creating the correspondence of a substitution portion with respect to each of signals in the description;

syntax analyzing means for creating a syntax analyzing tree based on the logic description;

invariable attribute setting means for setting an invariable attribute with respect to a signal whose correspondence has been created by the RTL description inputting means in the syntax analyzing tree;

partial circuit synthesizing means for logically optimizing a partial circuit except for a signal having the invariable attribute from the syntax analyzing tree so as to allocate the device model in the library;

invariable part optimizing means for inserting a buffer in order to satisfy a design rule with respect to the signal having the invariable attribute;

performance calculating means for calculating the performance of the integrated circuit; and

display means for displaying the result of the performance calculation and the logic description.

2. A system for estimating the performance of an integrated circuit in a register transfer level, in which

the performance of an integrated circuit is estimated based on a net list of a gate level including a signal having correspondence to a logic description of a register transfer level, the system for estimating the performance of an integrated circuit in a register transfer level comprising:

floorplan means for arranging a device model inside of the net list of the gate level within a specified region;

invariable part optimizing means for inserting a buffer based on arrangement information of the floorplan means in order to satisfy a design rule with respect to the signal having the correspondence to the logic description;

interconnection predicting means for predicting the interconnection between devices based on the arrangement information;

performance calculating means for calculating the performance of the net list of the gate level by the use of an interconnection prediction value by the interconnection predicting means; and

display means for displaying the result of the performance calculation, the logic description and the result of a floorplan.

3. A system for estimating the performance of an integrated circuit in a register transfer level as claimed in claim 1, further comprising delay recalculating means for creating the net list whose logic is optimized including the signal having the invariable attribute with respect to a selected path in accordance with a request from the outside, so as to calculate a delay of the path.

4. A system for estimating the performance of an integrated circuit in a register transfer level as claimed in claim 2, further comprising delay recalculating means

for creating the net list whose logic is optimized including the signal having the invariable attribute with respect to a selected path in accordance with a request from the outside, so as to calculate a delay of the path.

5. A system for estimating the performance of an integrated circuit in a register transfer level, in which the performance of an integrated circuit is estimated based on a net list of a gate level including a signal having correspondence to a logic description of a register transfer level, the system for estimating the performance of an integrated circuit in a register transfer level comprising:

display means for displaying a reach delay time of each of signals, which reaches a partial circuit on a net list of a gate level corresponding to a specified portion on the logic description.